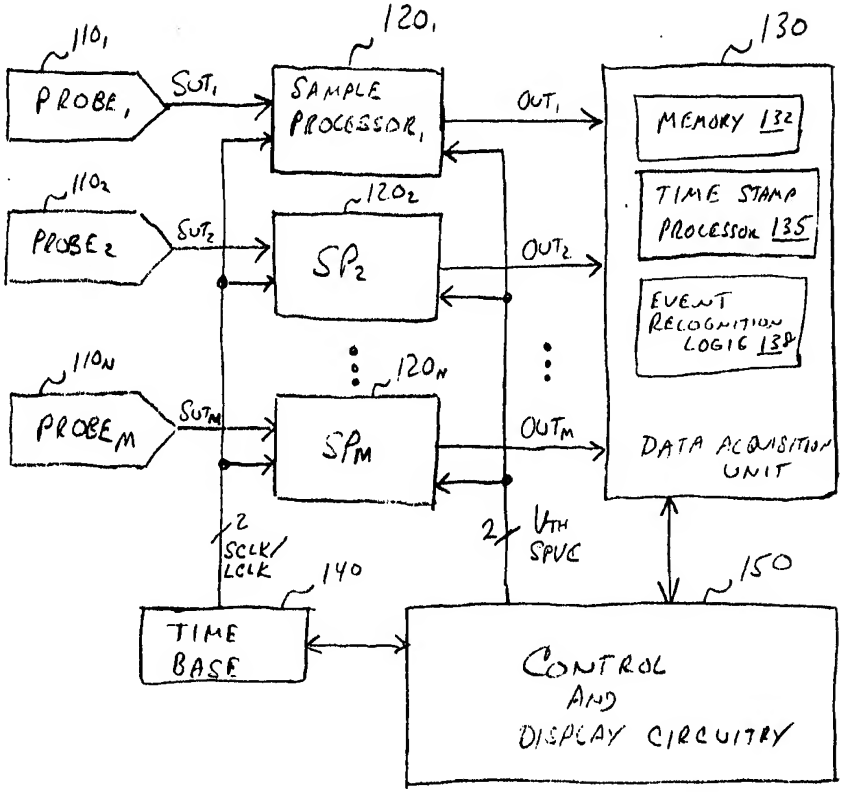

110₁
PROBE₁
SUT₁
120₁
SAMPLE PROCESSOR₁
OUT₁
130
MEMORY 132
TIME STAMP PROCESSOR 135
EVENT RECOGNITION LOGIC 138
110₂
PROBE₂
SUT₂
120₂
SP₂
OUT₂
110N
PROBEM
SUTM
120N
SPM
OUTM
DATA ACQUISITION UNIT
2
SCLK/LCLK
2
VTH SPVC
140
150
TIME BASE
CONTROL AND DISPLAY CIRCUITRY

100

FIG. 1

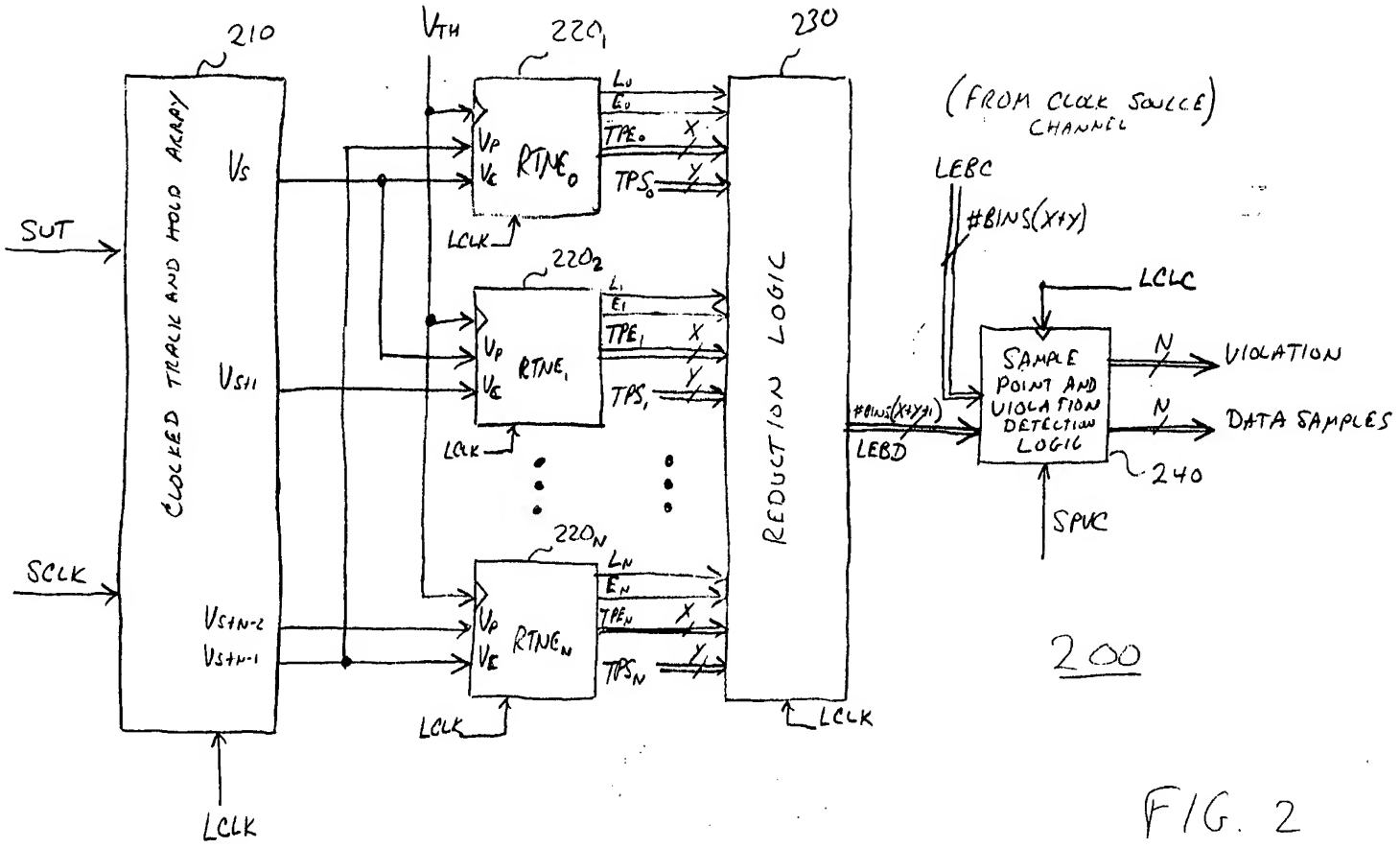
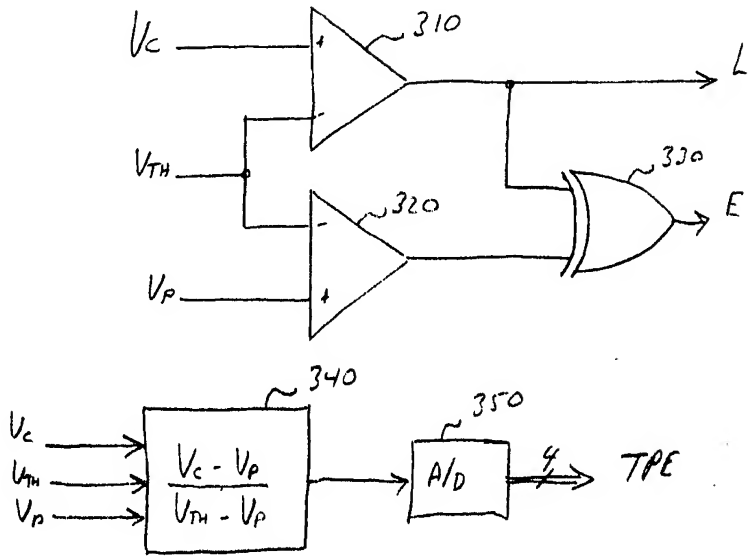
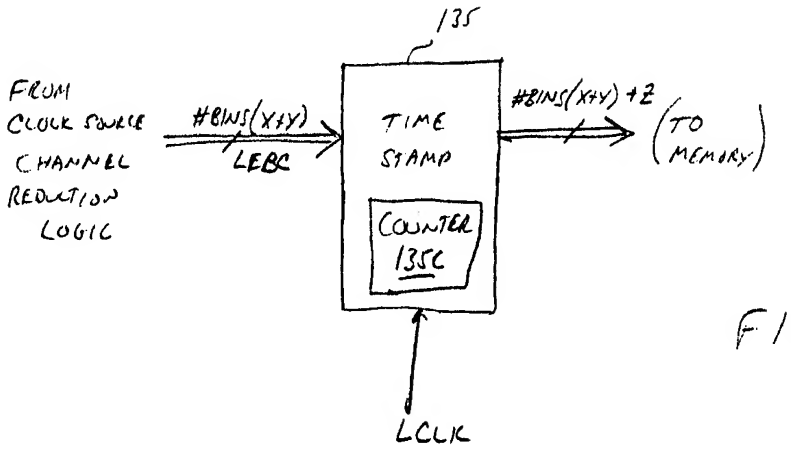

210
CLOCKED TRACK AND HOLD ARRAY
V_{TH}
220_1
220_2
220_N
230
V_S
V_{S+1}
V_{S+N-2}
V_{S+N-1}
SUT
SCLK
LCLK
V_P
V_E
$RTNE_0$
$RTNE_1$
$RTNE_N$
L_0
E_0
TPE_0
TPS_0
L_1
E_1
TPE_1
TPS_1
L_N
E_N
TPE_N
TPS_N
X
Y
REDUCTION LOGIC
(FROM CLOCK SOURCE)
CHANNEL
LEBC
#BINS(X+Y)
LCLC
SAMPLE POINT AND VIOLATION DETECTION LOGIC
240
N
VIOLATION
DATA SAMPLES
#BINS(X+Y+1)
LEBD
SPVC
200

FIG. 2


V_C
310
L
V_{TH}
320
330
E
V_P
340
350
V_C
V_{TH}
V_P
$\frac{V_C - V_P}{V_{TH} - V_P}$
A/D
4
TPE

300

FIG. 3



Z = LOGIC CLOCK #

FIG. 4

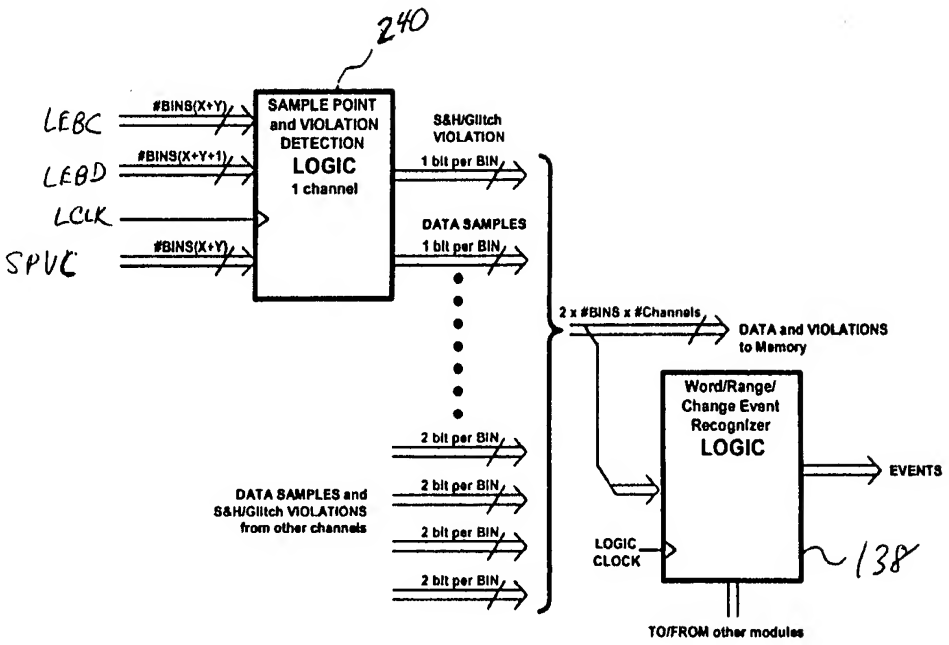

240
LEBC
LEBD
LCLK
SPVC
#BINS(X+Y)
#BINS(X+Y+1)
#BINS(X+Y)
SAMPLE POINT and VIOLATION DETECTION LOGIC 1 channel
S&H/Glitch VIOLATION
1 bit per BIN
DATA SAMPLES
1 bit per BIN
2 bit per BIN
2 bit per BIN
2 bit per BIN
2 bit per BIN
DATA SAMPLES and S&H/Glitch VIOLATIONS from other channels
2 x #BINS x #Channels
DATA and VIOLATIONS to Memory
Word/Range/ Change Event Recognizer LOGIC
EVENTS
LOGIC CLOCK
138
TO/FROM other modules

FIG. 5

Edge Detection - CLOCK channel

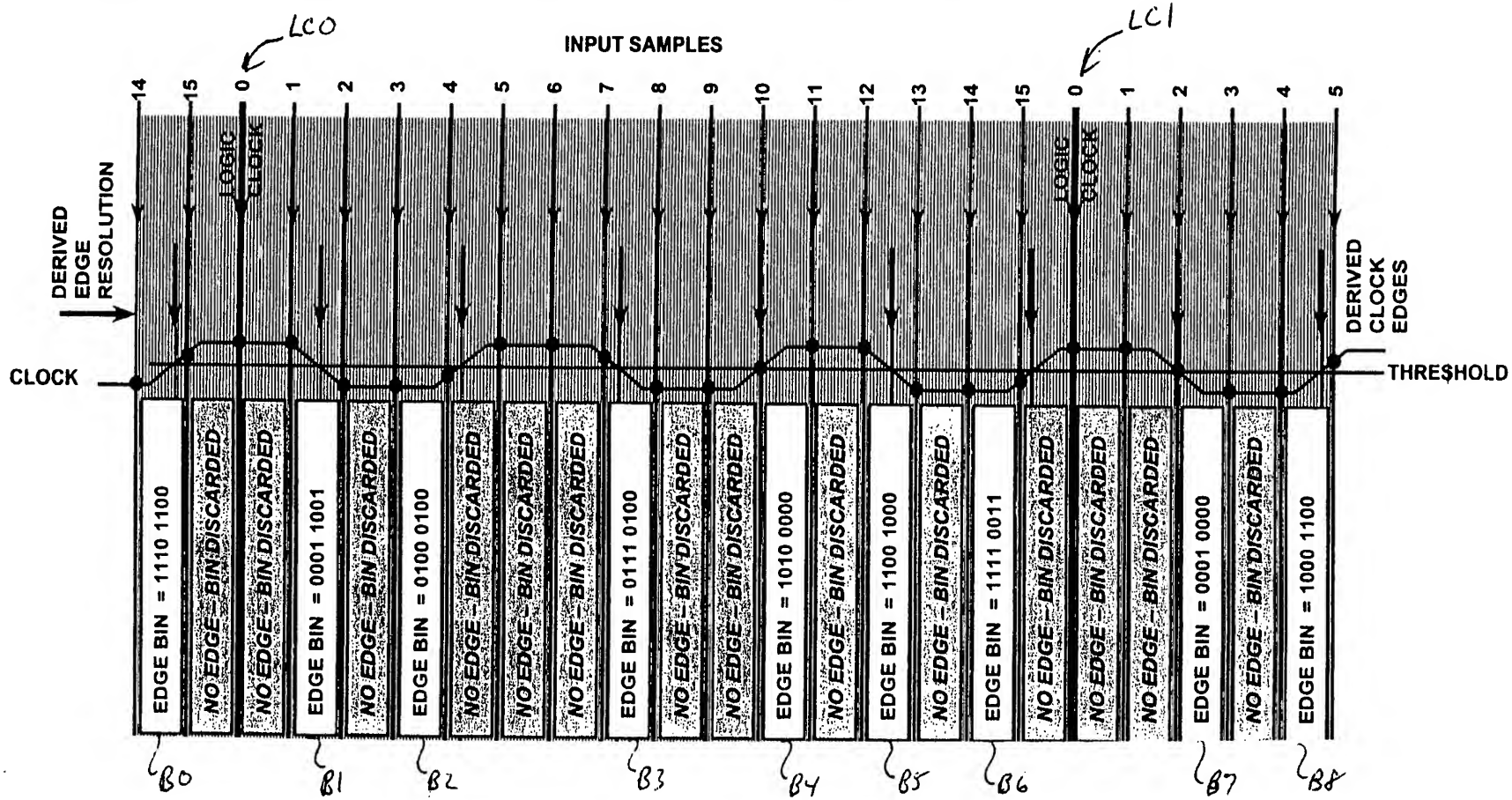


FIG. 6

Sample Point Detection

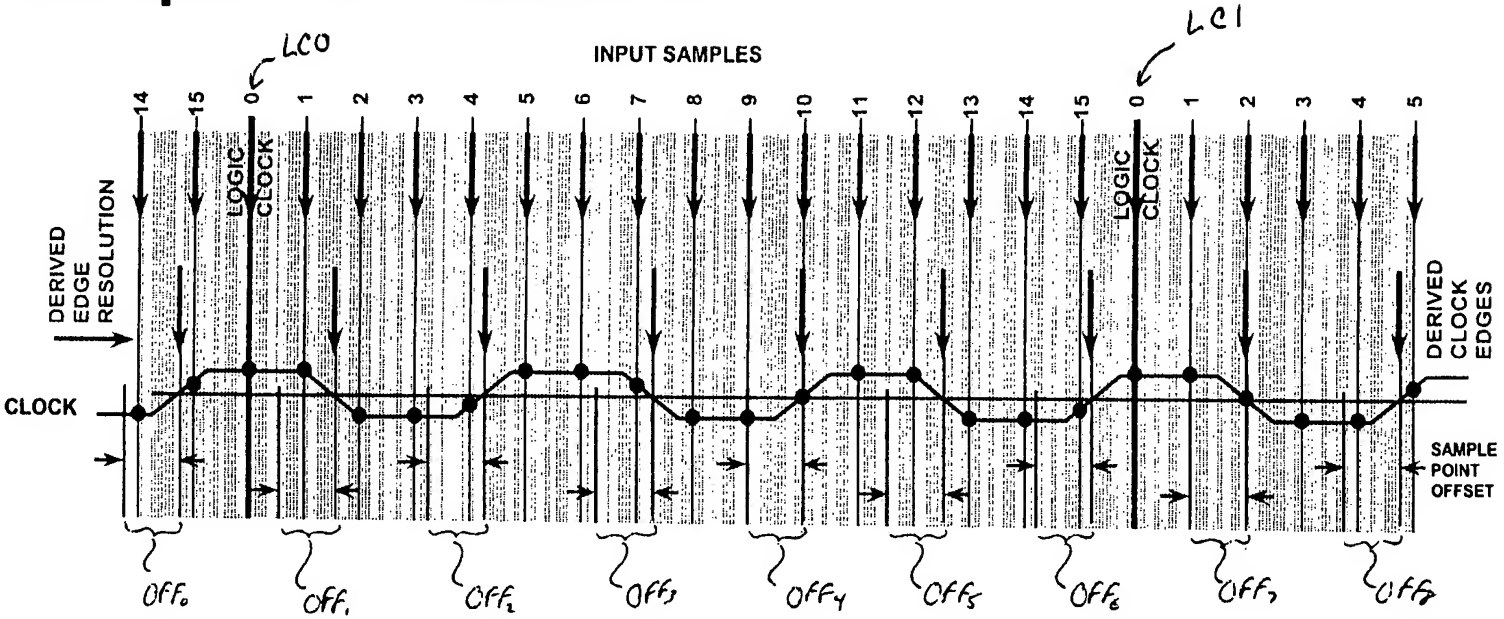


FIG. 7

Edge Detection - DATA channel

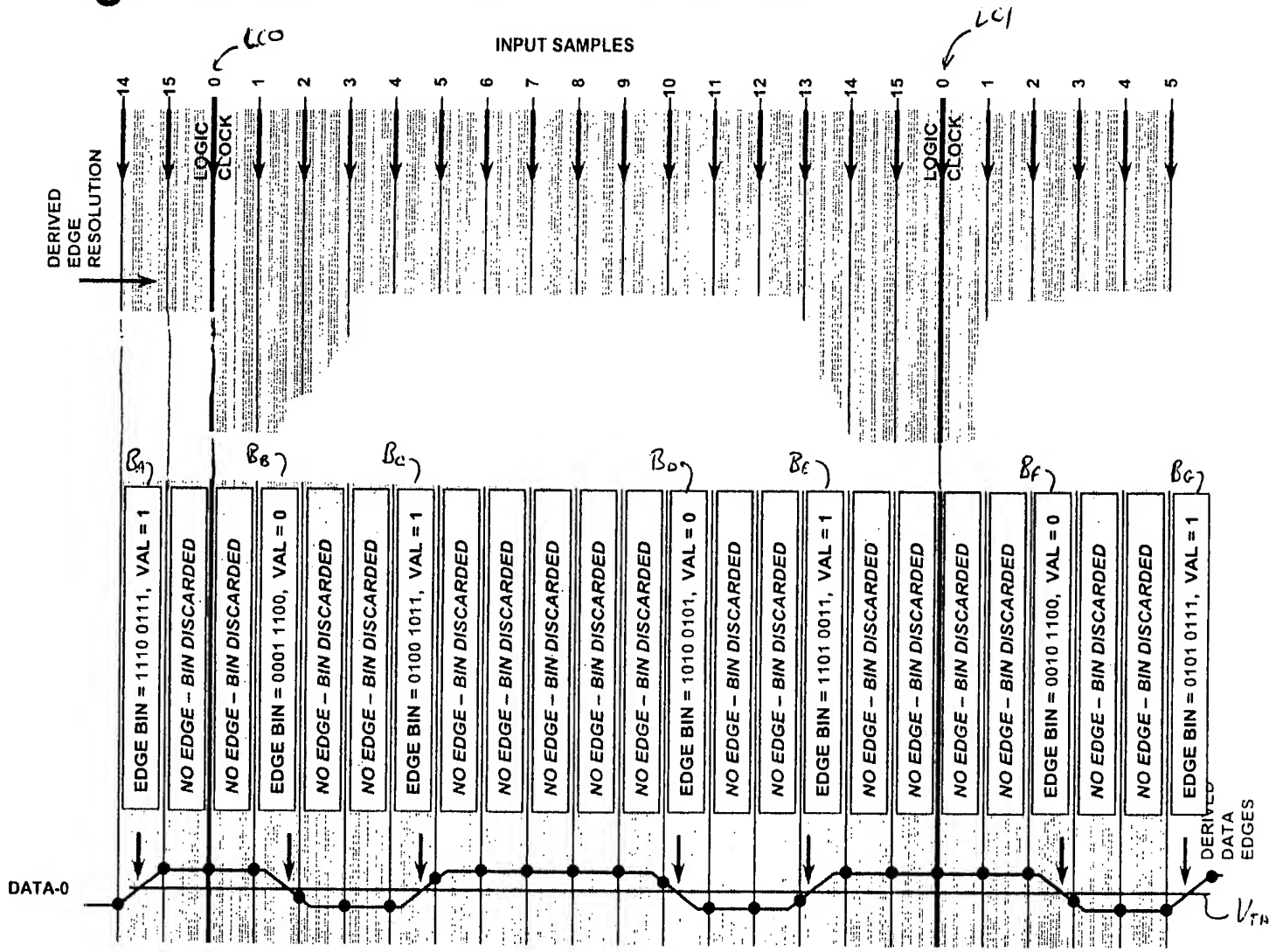


FIG. 8

Sample Point Detection

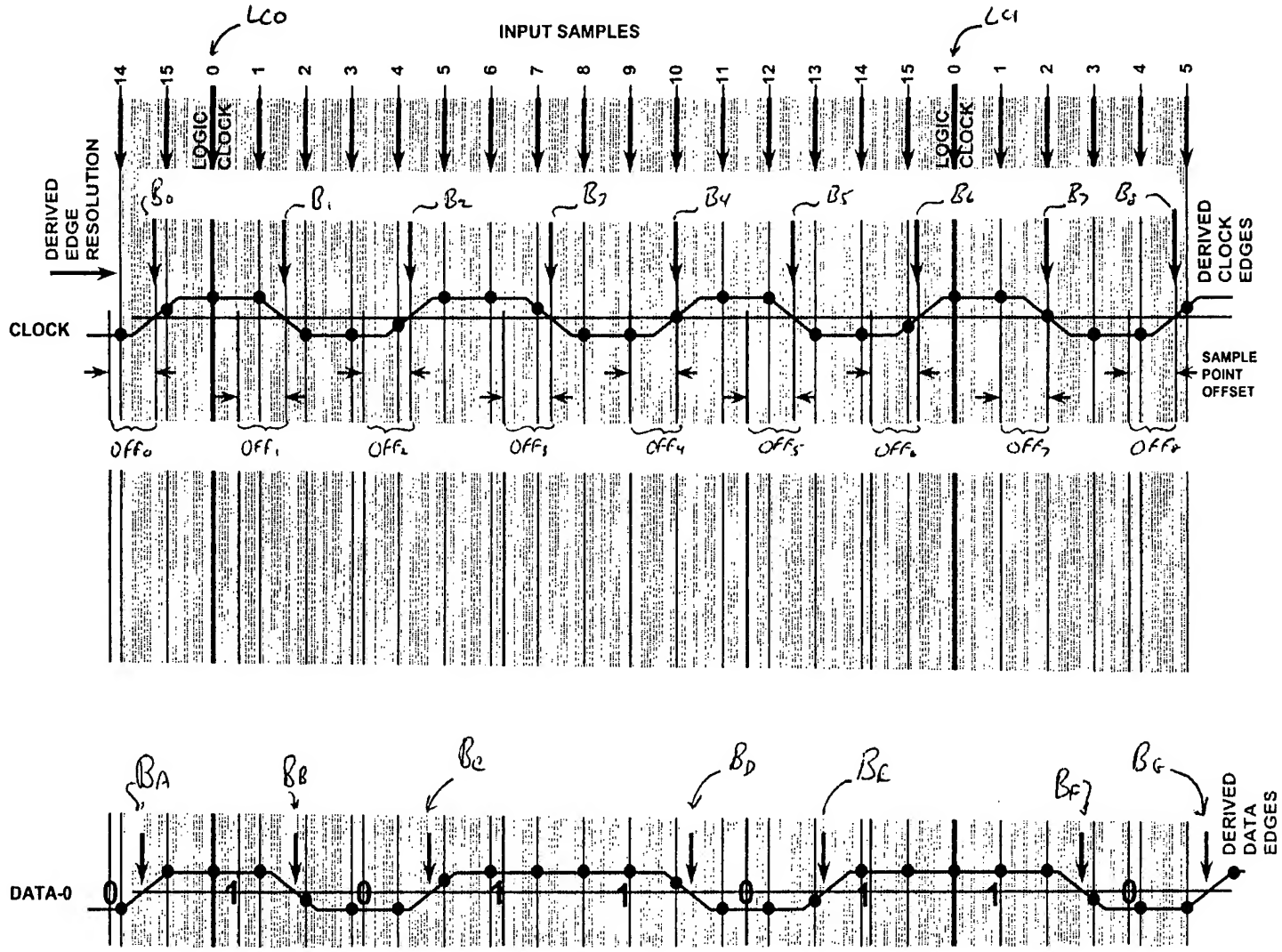
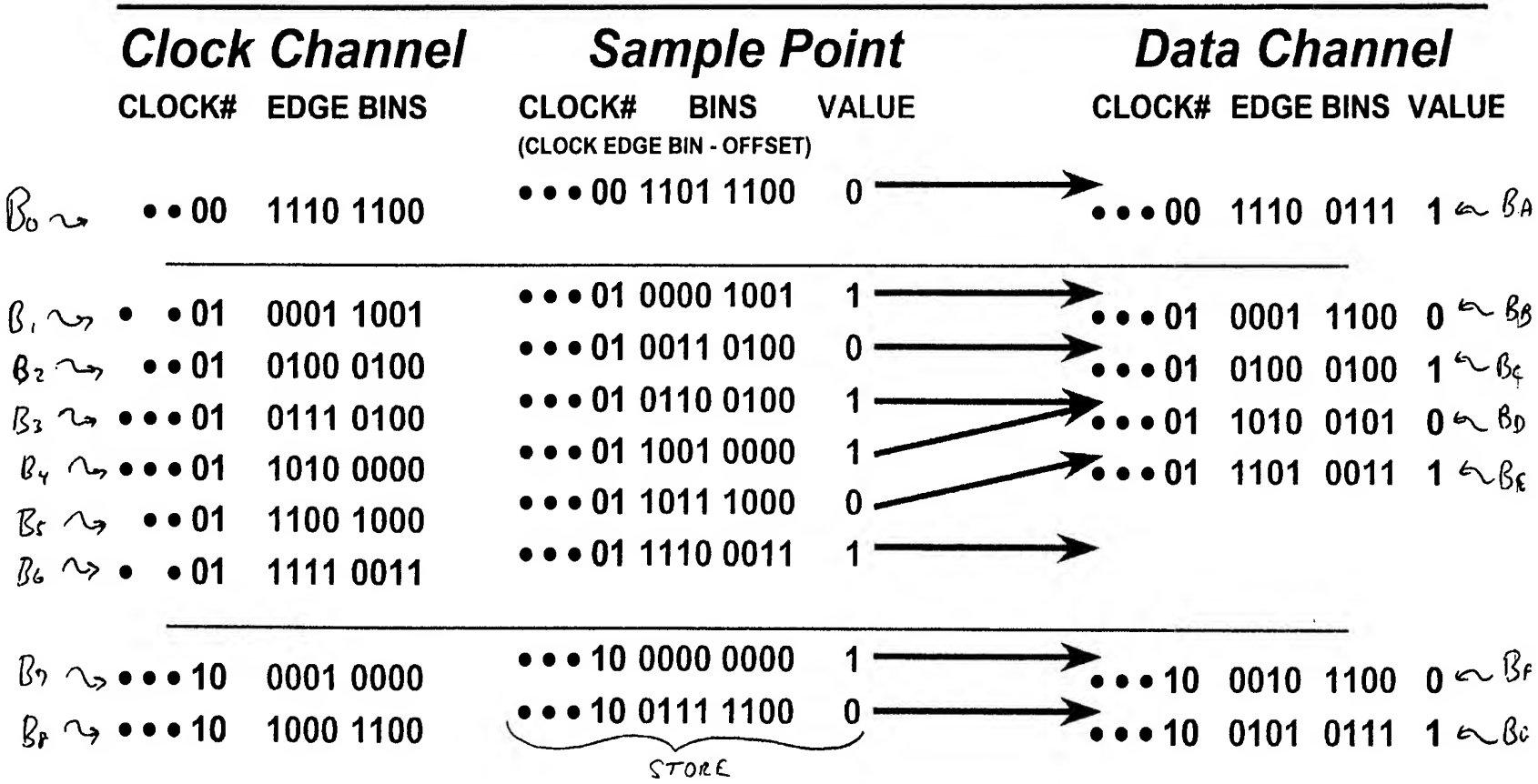


FIG. 9

Sample Point Detection - all channels



Sample point is 100 ps before clock edge
(sample point bin = clock edge bin - 0001 0000)

FIG. 10